UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT(S)	Jean-Michel Reynes et al	GROUP ART UNIT:	2814
APPLN. NO.:	10/518,158	EXAMINER:	John C. Ingham
FILED:	December 10, 2004		
TITLE:	POWER SEMICONDUCTOR DEVICE WITH A BASE REGION AND METHOD OF MANUFACTURING THE SAME		

Certificate of Submission

I hereby certify that this correspondence is being submitted to the U.S.P.T.O., Alexandria, VA.

☐ Addressed per C.F.R.§ 1.1(a) and deposited with the United States Postal Service with sufficient postage as first class mail.

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☒ Submitted electronically via EFS in accordance with "Legal Framework for EFS Web".

August 21, 2007
Date of Submission

/Stacie Herrera/
Signature

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Printed Name of Person Signing Certificate

APPEAL BRIEF

HONORABLE COMMISSIONER FOR PATENTS
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BOARD OF PATENT APPEALS & INTERFERENCES:

SIR:

Applicants file this brief with the Board of Appeals and Interferences regarding the appeal of the rejected claims in the above-referenced patent application.

REAL PARTY IN INTEREST

The present application is wholly assigned to FREESCALE SEMICONDUCTOR, INC., with its headquarters in Austin, Texas.

RELATED APPEALS AND INTERFERENCES

Appellants are unaware of other appeals or interferences which will directly affect, be directly affected by, or have a bearing on the Board's decision in this appeal.

STATUS OF CLAIMS

Claims 6-7, 10-11 and 14-16 are pending. Claims 1 to 14 were originally filed, claims 15 and 16 were added during prosecution, and claims 1 to 5, 8, 9, 12 and 13 were canceled during prosecution.

Claims 6-7, 10-11, and 15-16 stand rejected under 35 U.S.C. 103(a) over Neilson, US Patent No. 5,399,892 (Neilson) in view of Tsoi, US Patent No. 5,631,484 (Tsoi). Claim 14 stands rejected under 35 U.S.C. 35 over Neilson and Tsoi in view of Knoch, US Patent No. 5,703,389 (Knoch).

STATUS OF ADMENDMENTS

In the Statement of Reasons for Pre-Appeal Brief Review, Applicants requested that an Examiner's amendment be made to amend claim 11 to depend from claim 10 instead of claim 0. Claim 10 is the only pending independent claim remaining. This amendment is being repeated in the Claims Appendix. Since this amendment is being made to correct an informality, Applicants respectfully request its admittance.

SUMMARY OF CLAIMED SUBJECT MATTER

Claim 10

The language of claim 10 (the only independent claim) will first be compared with the example of an embodiment as shown in Fig. 4 then as shown in Fig 5 of the drawings. The language of claim 10 expressly states (reference numerals corresponding to the drawings having been added for the purpose of explanation of the example illustrated only):

"A method for manufacturing a power semiconductor device comprising:

forming a two-dimensional array of individual cells from a first surface (92) of a semiconductor substrate (62), each individual cell having source regions (37) within a single and substantially uniformly doped base region (36) surrounding said source regions of the individual cells of said array, and

forming a patterned insulated gate region (32) at said first surface,

...

wherein forming said single and substantially uniformly doped base region (36) comprises the steps of:

using said patterned insulated gate region (32) in forming a plurality of base region branches (80) extending radially towards at least one base region branch (80) of an adjacent cell to present juxtaposed base region ends, ..."

The process steps thus far in the language of claim 10 result in the production of an unfinished device as shown in annotated Fig.4 as set forth below, which is a partial plan view of a device having an array of cells of which nine appear at least partially in Fig. 4, out of a total of several hundred thousand that the array may include on a single die. Fig. 4 shows the die with the gate region 32 partly cut away at 34 to show the underlying base region branches.

Figure 4 set forth below has been annotated to show the base regions 36 in cross hatch prior to the "subsequently merging" step (set forth below) of claim 10 so as to highlight how the base regions are affected by the subsequently merging step. As will be set forth later, none of the cited prior art teach the "subsequently merging" step.

The finished cells have respective separate source regions 37 and a common drain region 39. At the stage of the process shown in Fig. 4, each cell of the array has a separate individual base region 36 (also referred to in the specification as a well region or a PHV/NHV or a body region). Each separate individual base region 36 in this example comprises four branches 80, the base regions within the cut-away area 34 of the gate being identified by the cross hatching in the following annotated copy of Fig. 4.

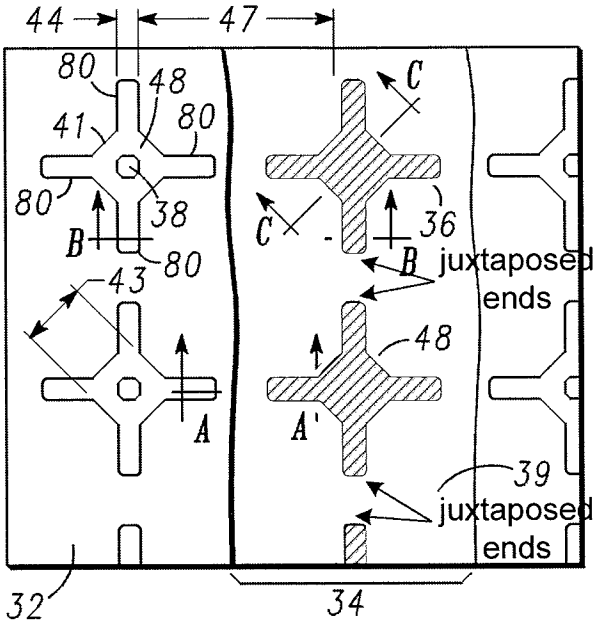

FIG. 4

Juxtaposed base regions ends are identified in writing between adjacent cells that are spaced vertically in the drawing; similar juxtaposed ends occur between adjacent cells that are spaced horizontally in the drawing, of course.

Claim 10 specifies an additional "subsequently merging" step, used in the production of the device structure as shown in Fig.5:

> "subsequently merging together the base region branches (80) of adjacent cells adjacent and between said juxtaposed base region ends to form said single and substantially uniformly doped base region."

As a result of one embodiment of the subsequently merging step, the base regions 36, which were separate are merged as shown by the cross hatching in the following annotated copy of Fig. 5. It will be seen that the separate individual base regions at the stage shown in Fig. 4, which laterally were the size of the corresponding openings in the gate layers, have now spread laterally so as to merge between the juxtaposed ends of the branches 80 of adjacent cells and also adjacent the base region ends and elsewhere, becoming a single common base region 36. The source regions 37 are formed after the formation of the base region 36. In the completed cells, the merged base region 36 extends beneath all the source regions 37 of the cells of the array, so that it surrounds all the source regions in the thickness of the substrate. The drain region 39 still extends underneath the merged base region 36 but now only appears at the surface 92 of the die in separate areas identified in writing in the following copy of Fig. 5. The dopant transitions at the surface 92 between the drain region and the base region are covered by the gate 32, which

also covers the dopant transitions between the source regions 37 and the common base region 36 to control the current flow, as described on page 16 lines 27-32 of the specification.

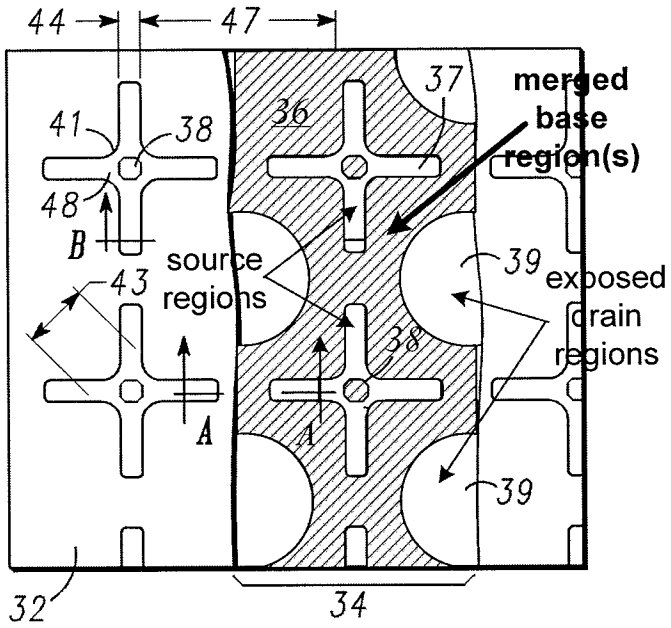

FIG. 5

Page 13, lines 10-21 of the present application sets forth an embodiment for forming a base region where the PHV dopant is merged right after implantation. In that embodiment, merging is accomplished by subjecting the cells to a temperature of 1100 C for 1-2 hours after implantation of the base dopant.

GROUNDS FOR REJECTION TO BE REVIEWED ON APPEAL

1. Are claims 6-7, 10-11, and 14-16 unpatentable under 35 U.S.C § 103 in view of Neilson, Tsoi and Knoch?

ARGUMENTS

Claim 10 has been rejected under 35 U.S.C. 103(a) as being unpatentable over Neilson in view of Tsoi in the Office Action dated January 24th 2007, confirmed in the advisory action of May 8th 2007. This rejection is being traversed at least for the reasons set forth below.

Neither Neilson nor Tsoi, either alone or in combination teach "subsequently merging together the base region branches of adjacent cells adjacent and between said juxtaposed base region ends to form said single and substantially uniformly doped base region," all as recited by independent claim 10.

Regarding Neilson

Referring to paragraph 6 of the Office Action dated January 24th 2007, the Examiner agrees that Neilson does not disclose the process step of subsequently merging together the base region branches of adjacent cells adjacent and between said juxtaposed base region ends to form said single and substantially uniformly doped base region as set forth by Claim 10. Instead, Neilson photo-masks the body regions for implantation and strips the mask prior to depositing the gate insulators and electrodes.

Regarding Tsoi

The Office Action of January 24th 2007 points out that Tsoi produces self-aligned base and source regions with a reduced number of masking steps. However, this Office Action then states: "A subsequent diffusion and activating merges the dopant between juxtaposed base contacts (column 4, line 7-9).

It is respectfully submitted that Tsoi does not teach subsequently merging together the base region branches of adjacent cells adjacent and between said juxtaposed base region ends to form said single and substantially uniformly doped base region as claimed in present claim 10.

In the Examiner's comments of May 8th 2007, the Examiner states: "the Tsoi reference teaches patterning insulated gate regions to form a plurality of implanted base region branches with juxtaposed ends then diffusing the branches. As seen in the reference Fig 1, the branches (19) are merged together to form a single and substantially uniform doped base region."

Applicants respectfully submit that this above statement regarding Tsoi by the Examiner is erroneous.

The passage at column 4, lines 7-9 of Tsoi reads: "After implantation, the implanted dopant is diffused and activated using an appropriate anneal cycle." There is no reference to "merges the dopant between juxtaposed base contacts" as the Examiner states. Figure 1 of Tsoi is a "top view of a portion of a power MOSFET device suitable for manufacture using" the invention of Tsoi (column 1 lines 44-46); it shows stripes 11-17 each comprising dumb-bell and narrowed portions 18 & 19, whose manufacturing process is described with reference to Figs 3-13, notably Figs 3-5.

As described in column 3, lines 23 to 25, Fig 3 of Tsoi shows substrate 26 after a dielectric layer or interlayer dielectric 37 is formed over polycrystalline gate layer 34. As described column 3 lines 39 to 52, a protective photo-mask layer 42 is formed over dielectric layer 37, exposed portions of dielectric layer 37 and polycrystalline gate layer 34 are etched to provide formed openings 143 and 144 shown in Fig 4, which shows insulated gate regions 122 and 222 separated by dumb bell portion 18 and stripe portion 19. As described in column 3 lines

58 to 63, next, doped base regions 47 are formed extending into substrate 26 (using ion implantation) and are self-aligned to insulated gate portions 122 and 222.

As described column 4, lines 7 to 11, the structure shown in Fig 4 of Tsoi is provided after implantation by diffusion and annealing. Doped base regions 47 are clearly shown separated in Figs 4 & 5, after the diffusion and annealing. These regions are not subject to a process step of merging regions of adjacent cells and do not form a single and substantially uniformly doped base region as set forth by Claim 10. Instead, the stripes are stated to be separated (column 2 lines 24-25).

The stripes 11 to 17 of Fig 1, including dumb bell portions 18 and stripe portions 19, are produced by the self-aligning photo-mask, etch and implantation steps shown in Figs 3 and 4, not by merging juxtaposed edges or ends of the base regions. Never does Tsoi refer to merging base portions of adjacent cells, as claimed in present claim 10. If the equivalents of 'adjacent cells' in Tsoi are the stripes 11 to 17, and if dumbbell and stripe portions 18 and 19 are to be considered as juxtaposed, as seen in Tsoi Fig 4 and subsequent Figures, they always remain 'juxtaposed', that is to say separated, and never merged. This is clearly seen from the following annotated copy of **FIG. 5 OF TSOI**, in which the separate base regions are identified by cross hatching.

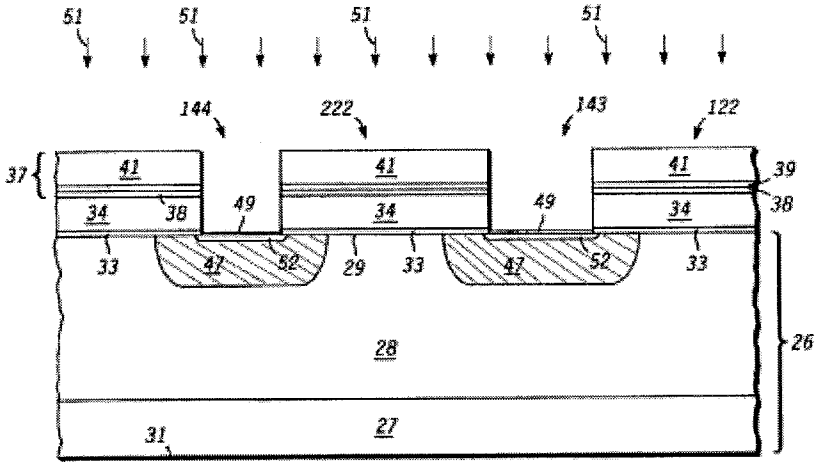

FIG. 5

As can be seen from the above Figure and from the cited portions of its specification, Tsoi just does not teach subsequently merging together the base region branches of adjacent cells adjacent and between said juxtaposed base region ends to form said single and substantially uniformly doped base region.

Regarding Knoch

Analogous comments apply to Knoch, who does not teach merging base portions of adjacent cells either.

CONCLUSIONS

As stated above Neilson, Tsoi, and Knoch do not disclose "subsequently merging together the base region branches of adjacent cells adjacent and between said juxtaposed base region ends to form said single and substantially uniformly doped base region."

Because none of the references teach the above cited "subsequently merging" step, the obviousness rejection of claim 10 should be removed in that a prima facie case of obviousness has not been met with respect to claim 10. Please see MPEP Section 2143.03 where it states "To establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art."

The formation of a common merged base region may give advantages that are not obtained by the devices made by the processes described by Neilson, Knoch or Tsoi or any combination of their teachings. As described in the present application on page 12, lines 16-21 "By having merged well or PHV" *(base)* "regions, the phenomenon of parasitic NPN or PNP bipolarity (also called snap back effect) is avoided since the base region will always be polarised, which is a major improvement. Thus, the breakdown voltage is improved as well as the Unclamped Inductive Switching (UIS) such that the voltage and the current circulating between the individual cells can be sustained at a higher level."

Accordingly, it is submitted that the distinctions described above between the teachings of the cited art and claim 10 are not obvious, and therefore Claim 10 is allowable.

The dependent claims each depend from claim 10 are allowable for at least the same reasons given for the independent claim.

Accordingly, it is submitted that all the claims are allowable and issue of a patent on the application is solicited.

Respectfully submitted,

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Claims Appendix

1. – 5. (Canceled)

6. (Previously Presented) The method for manufacturing a power semiconductor device according to claim 10, wherein the device comprises at least one drain electrode contacting a face of said semiconductor substrate opposite said source regions.

7. (Previously Presented) The method for manufacturing a power semiconductor device according to claim 6, wherein the device comprises physically isolated drain regions in the substrate and wherein said physically isolated drain regions have a depth equivalent to the depth of said base regions.

8. – 9. (Canceled)

10. (Previously Presented) A method for manufacturing a power semiconductor device comprising:

forming a two-dimensional array of individual cells from a first surface of a semiconductor substrate, each individual cell having source regions within a single and substantially uniformly doped base region surrounding said source regions of the individual cells of said array, and

forming a patterned insulated gate region at said first surface, wherein the source regions of the individual cells of the array comprise a plurality of source region branches each extending towards at least one source region branch of an adjacent cell, the source region branches of adjacent cells presenting juxtaposed ends, wherein forming said single and substantially uniformly doped base region comprises the steps of:

using said patterned insulated gate region in forming a plurality of base region branches extending radially towards at least one base region branch of an adjacent cell to present juxtaposed base region ends,

subsequently merging together the base region branches of adjacent cells adjacent and between said juxtaposed base region ends to form said single and substantially uniformly doped base region.

11. (Currently Amended) The method for manufacturing a power semiconductor device as claimed in claim ~~9~~ 10 comprising the steps of:

using said patterned insulated gate region in forming said source region within each base region of each individual cell with said radially extending source region branches corresponding to said base region branches.

12. – 13. (Canceled)

14. (Previously Presented) The method of manufacturing a power semiconductor device according to claim 10 wherein forming said base regions comprises a step of using said patterned insulated gate region in making ion implant of high voltage breakdown resistance for the base region branches before merging together the base region branches.

15. (Original) The method of manufacturing a power semiconductor device according to claim 10, wherein forming said base region comprises the step of causing the base region branches of adjacent cells to diffuse laterally of the array so as to merge together adjacent and between said juxtaposed ends.

16. (Original) The method of manufacturing a power semiconductor device according to claim 10, wherein said source regions are formed after merging said base region branches.

Evidence Appendix

There is no information needed to be presented in this appendix.

Related Proceedings Appendix

There is no information needed to be presented in this appendix.